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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/334,646	06/17/1999	SHUNPEI YAMAZAKI	0756-1984	5565
31780	7590	01/05/2006		EXAMINER
ERIC ROBINSON			HU, SHOUXIANG	
PMB 955				ART UNIT
21010 SOUTHBANK ST.				PAPER NUMBER
POTOMAC FALLS, VA 20165			2811	

DATE MAILED: 01/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/334,646	YAMAZAKI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1,2,11-14,16,38-41,58,59,71,72,78,79,100,101 and 122-145 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_ is/are allowed.
- 6) Claim(s) 1,2,11-14,16,38-41,58,59,71,72,78,79,100,101 and 122-145 is/are rejected.
- 7) Claim(s) \_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. ____ .
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>12/5/05, 6/15/05</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: ____ .

## DETAILED ACTION

### ***Claim Objections***

1. Claims 1-2, 11-14, 16, 38-41, 58-59, 71-72, 78-79, 100-101 and 122-145 are objected to because of the following informalities and/or defects:

Claims 1-2, 122, 128, 134 and 140 each recite or implicate the subject matters that the channel-forming regions of the recited two transistors are in two separated semiconductor layers. However, among various possible interpretations, such limitations may be interpreted as meaning: the two transistor for formed of two different semiconductor layers (on different levels), even though they may both be formed in contact with a same insulating surface. For example, two separated film layers may be displaced on two different levels but can still be in contact with a same insulation layer that has an uneven or tilt surface. It would then be unreadable on the specification and the drawings (see Fig. 3) of the instant disclosure, since the channel regions of the two transistors therein are formed of two separated regions of a same semiconductor layer. Accordingly, the recited “semiconductor layer” should read as: --semiconductor region--, order to avoid potential confusions.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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3. Claims 1-2, 11-14, 16, 71-72, 78-79, 122-125, 127-131, 133-137, 139-143 and 145 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiroyoshi (JP 6-123896, May, 1994; of record).

Hiroyoshi discloses an active matrix type LC display device having a buffer circuit (2 and 3; here the drive portion of 3 is regarded as a part of the buffer circuit 2 and 3, as it naturally functions as a switching element for the buffered signals) in the drive circuit (1, 2 and 3), comprising: first and second TFTs (see Fig. 2), wherein the two TFTs share a common gate electrode, a common source electrode and a common drain electrode, and the two channel forming regions of the two TFTs are formed in separated regions of a Si layer that is naturally on and in contact with a same insulating surface, as the surface of the substrate has to be insulative, otherwise the TFTs would not be workable due to potential adverse shortening between the source/drain regions; and, wherein the two parallel-connected TFTs, along with their semiconductor layer or regions, are arranged in the channel width direction (see Fig. 2).

In addition, it is noted that an active matrix type LC device such as the one of Hiroyoshi naturally further comprises a memory and a decode. And the channel-forming regions in the thin Si film therein naturally have point defects, due to the naturally of the resulting silicon thin film.

Regarding claims 124, 130, 136 and 142, the common gate, source and drain electrodes for the two TFTs in Hiroyoshi are all extended in parallel with each other (see Fig. 2).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 38-41, 58-59, 100-101, 126, 132, 138 and 144, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyoshi in view of Zhang (US 5,403,772; of record).

The disclosure of Hiroyoshi is discussed as applied to claims 1-2, 11-14, 16, 71-72, 78-79, 122-125, 127-131, 133-137, 139-143 and 145 above.

Although Hiroyoshi does not expressly disclose that the silicon semiconductor layer can be monocrystalline, one of ordinary skill in the art would readily recognize that monocrystalline silicon can be desirably formed for improving the performance of the TFTs, as evidenced in Zhang as explained below.

Zhang teaches to form an active matrix type LC display device (Figs. 1-8A, particularly, Fig. 8A), comprising: a pixel matrix portion (104) having a plurality of pixels on an insulating substrate (107); and a peripheral driver circuit portion (101 and 102) on the same insulation substrate, thin film transistors (TFTs) in the driver circuit portion

each having a channel forming region in one of the separate semiconductor layers (11a and 11b) provided on an insulating surface, wherein the channel forming region is provided in a region which can be regarded as effectively monocrystalline silicon (see col. 6, lines 13-15); and, the channel forming region contains impurities (a type of point defects) of carbon, nitrogen and oxygen at a concentration less than  $10^{18} \text{ cm}^{-3}$ , which meets the limitation of each channel forming region "containing carbon and nitrogen at a concentration of  $5 \times 10^{18} \text{ cm}^{-3}$  or less, respectively, and containing oxygen at a concentration of  $5 \times 10^{19} \text{ cm}^{-3}$  or less" recited in the claimed invention. It is noted that, since the channel forming region in Zhang is formed with a method which is substantially the same as the one used in the claimed invention, the method used in Zhang is regarded as being inherently capable of forming the channel forming region having no linear defects or surface defects. In addition, one of ordinary skill in the art would readily recognize that it is always desirable to form the channel forming region having no linear defects or surface defects for achieving good channel performance.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the monocrystalline silicon layer of Zhang into the TFT device of Hiroyoshi, so that an active matrix type LC display with better TFT performance therein would be obtained.

### ***Response to Arguments***

5. Applicant's arguments with respect to the rejected claims above have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH  
January 3, 2006



SHOUXIANG HU  
PRIMARY EXAMINER